CLAIM AMENDMENTS

Claims pending:

- At time of the Office Action: Claims 1-29.
- After this Response: Claims 1-29.

Cancelled claims: none.

Amended claims: none.

New Claims: none.

The status of the Claims is as follows:

1. **(Original)** An apparatus comprising:

a circuit board having front and back surfaces;

at least one memory device having a plurality of pins mounted on the front surface of the circuit board;

at least one other memory device having a plurality of pins mounted on the back surface of the circuit board;

said memory devices being mounted on the circuit board such that at least some pins from the one memory device align with at least some pins of the other memory device to provide aligned pin pairs; and

a via disposed in the circuit board and extending between and connecting individual pins of an aligned pin pair.

2. **(Original)** The apparatus of claim 1 further comprising multiple vias disposed in the circuit board and extending between and connecting individual pins of different aligned pin pairs.

3. **(Original)** The apparatus of claim 2, wherein at least some via-connected pins comprise address pins.

4. **(Original)** The apparatus of claim 2, wherein at least some via-connected pins comprise control pins.

5. **(Original)** The apparatus of claim 2, wherein at least some via-connected pins comprise address pins and other via-connected pins comprise control pins.

6. **(Original)** The apparatus of claim 1, wherein said via-connected pins comprise address pins.

7. **(Original)** The apparatus of claim 1, wherein said via-connected pins comprise control pins.

8. **(Original)** The apparatus of claim 1, wherein said memory devices define a footprint on the circuit board, and further comprising one or more termination resistor packs operably coupled with at least one memory device for terminating data signals associated with a memory device, said one or more termination resistor packs being mounted on the circuit board on a surface opposite of the surface on which its associated memory device is mounted, said one or more termination resistor packs being mounted within the footprint of the associated memory device.

9. **(Original)** The apparatus of claim 1, wherein said memory devices define a footprint on the circuit board, and further comprising one or more decoupling capacitors operably coupled with at least one memory device, said one or more decoupling capacitors being mounted on the circuit board on a surface opposite of the surface on which its associated memory device is mounted, said one or more decoupling capacitors being mounted within the footprint of the associated memory device.

10. **(Original)** A computer system embodying the apparatus of claim 1.

11. (Original) An apparatus comprising:

a circuit board having front and back surfaces;

a first plurality of memory devices, each memory device having a plurality of address pins and control pins mounted on the front surface of the circuit board;

a second plurality of memory devices, each memory device having a plurality of address pins and control pins mounted on the back surface of the circuit board;

said memory devices being configured in a dual bank configuration;

said memory devices being mounted on the circuit board such that at least some address and control pins from a front surface mounted memory device share individual respective vias with at least some corresponding address and control pins of a back surface-mounted memory device;

a memory controller mounted on the circuit board and operably connected with the first and second plurality of memory devices;

wherein a first group of address pins are interconnected with the memory controller using a first topology and a second group of address pins are interconnected with the memory controller using a second different topology.

12. (Original) The apparatus of claim 11, wherein the memory devices comprise dual row, gull wing-type devices.

13. (Original) The apparatus of claim 11, wherein said memory devices define a footprint on the circuit board, and further comprising one or more termination resistor packs operably coupled with at least one memory device for terminating data signals associated with a memory device, said one or more termination resistor packs being mounted on the circuit board on a surface opposite of the surface on which its associated memory device is mounted, said one or more termination resistor packs being mounted within the footprint of the associated memory device.

14. (Original) The apparatus of claim 11, wherein said memory devices define a footprint on the circuit board, and further comprising one or more decoupling capacitors operably coupled with at least one memory device, said one or more decoupling capacitors being mounted on the circuit board on a surface opposite of the surface on which its associated memory device is mounted, said one or more decoupling capacitors being mounted within the footprint of the associated memory device.

15. (Original) A computer system embodying the apparatus of claim 11.

16. **(Original)** An apparatus comprising:

a circuit board having front and back surfaces;

at least one memory means mounted on the front surface of the circuit board, said memory means comprising address means and control means;

at least one other memory means mounted on the back surface of the circuit board, said other memory means comprising address means and control means;

means extending through the circuit board and operably connecting individual address means and control means from the one memory means with individual address means and control means from the other memory means;

said means extending through the circuit board being shared between individual respective address means and control means.

17. **(Original)** The apparatus of claim 16, wherein said memory means define individual footprints on the circuit board, and further comprising one or more termination means operably coupled with at least one memory means for terminating data signals associated with a memory means, said one or more termination means being mounted on the circuit board on a surface opposite of the surface on which its associated memory means is mounted, said one or more termination means being mounted within the footprint of the associated memory means.

18. **(Original)** The apparatus of claim 16, wherein said memory means define a footprint on the circuit board, and further comprising one or more decoupling means operably coupled with at least one memory means, said one or more decoupling means being mounted on the circuit board on a surface opposite of the surface on which its associated memory means is mounted, said one or more decoupling means being mounted within the footprint of the associated memory means.

19. **(Original)** A method comprising:

providing a circuit board having front and back surfaces;

mounting a first plurality of memory devices on the front surface of the circuit board, each memory device having a plurality of address pins and control pin; and

mounting a second plurality of memory devices on the back surface of the circuit board, each memory device having a plurality of address pins and control pins;

said acts of mounting being sufficient such that at least some address and control pins from a front surface-mounted memory device share individual respective vias with at least some corresponding address and control pins of a back surface-mounted memory device.

20. **(Original)** The method of claim 19 further comprising mounting a memory controller on the circuit board, the memory controller being operably connected with the first and second plurality of memory devices.

21. **(Original)** The method of claim 19, wherein said acts of mounting comprise mounting memory devices on the circuit board in a single bank configuration.

22. **(Original)** The method of claim 19, wherein said acts of mounting comprise mounting memory devices on the circuit board in a dual bank configuration.

23. **(Original)** The method of claim 19, wherein the memory devices comprise dual row, gull wing-type devices.

24. **(Original)** The method of claim 19, wherein said acts of mounting comprise mounting memory devices on the circuit board in an interconnected branched-t topology.

25. **(Original)** The method of claim 19, wherein said acts of mounting comprise mounting memory devices on the circuit board in a daisy-chained topology.

26. **(Original)** The method of claim 19, wherein said acts of mounting comprise mounting SDRAM devices on the circuit board.

27. **(Original)** The method of claim 19, wherein said acts of mounting comprise mounting DDR SDRAM devices on the circuit board.

28. **(Original)** The method of claim 19, wherein said memory devices define a footprint on the circuit board, and further comprising mounting one or more termination resistor packs on the circuit board and operably coupled with at least one memory device for terminating data signals associated with a memory device, said one or more termination resistor packs being mounted on the circuit board on a surface opposite of the surface on which its associated memory device is mounted, said one or more termination resistor packs being mounted within the footprint of the associated memory device.

29. **(Original)** The method of claim 19, wherein said memory devices define a footprint on the circuit board, and further comprising mounting one or more decoupling capacitors on the circuit board and operably coupled with at least one memory device, said one or more decoupling capacitors being mounted on the circuit board on a surface opposite of the surface on which its associated memory device is mounted, said one or more decoupling capacitors being mounted within the footprint of the associated memory device.